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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,391	04/19/2004	Hideki Takahashi	252069US2	9709

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,391	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-17* is/are pending in the application.

4a) Of the above claim(s) *7-12,16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Newly present claims 12, 16, and 17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on July 5, 2005. Note that claims 12 and 16 are drawn to Species III (Figure 11), while claim 17 is drawn to Species IV (Figure 12).

This application contains claims 7-12, 16, and 17 drawn to an invention or species nonelected with traverse in the response filed July 5, 2006. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 6, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. ("Effects of Shorted...", hereinafter Akiyama) in view of Tanaka (US PGPub 2001/0040255, hereinafter Tanaka).

Regarding claims 2 and 3, Figure 1a of Akiyama discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom); an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate; a first main electrode (emitter electrode) formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a first semiconductor layer (n+ short region) of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer (p+ collector region) of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and a second main electrode (collector electrode) formed on said first semiconductor layer and said second semiconductor layer; wherein an interface between said second main electrode and each of said first and second semiconductor layers is parallel to said first main surface; a first interface between said first semiconductor layer (n+ short region) and said second main electrode occupies approximately 50% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer; and a second interface between said second semiconductor layer (p+ collector region) and said second main electrode occupies approximately 50% of said interface between said second main electrode and each of said first

semiconductor layer and said second semiconductor layer. The difference between Akiyama and the claimed invention is a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 microns or smaller. Figure 10 of Tanaka discloses an IGBT with first and second semiconductor regions (12 and 2B, respectively) in a second main surface of a semiconductor substrate 1, wherein the thickness of the second semiconductor region 2B is less than 1 micron (approximately 0.8 microns) (paragraph [0187]). As shown in Figure 10, region 12 is thinner than region 2B, therefore the first semiconductor region 12 is also less than 1 microns. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akiyama by using a thickness of less than 1 micron for the first and second semiconductor regions as taught by Tanaka. The ordinary artisan would have been motivated to modify Akiyama in the manner described above for the purpose of reducing the carrier injection coefficient and increasing the turn-off speed of the device (paragraph [0190] of Tanaka). Furthermore, when the thickness of the first and second semiconductor regions as taught by Tanaka is incorporated into the device of Akiyama, the distance between said first main surface and said interface is 200 microns or smaller (190 microns + 0.8 microns).

Regarding claims 4 and 13, Figure 1a of Akiyama discloses a total width of a first width (W_n) of said first semiconductor layer (n+ short region) and a second width (W_p) of said second semiconductor layer (p+ collector region) which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is 120 microns (see Table 1, sample A).

Regarding claims 6 and 15, Figure 1a of Akiyama discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 1a of Akiyama has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama in view of Tanaka as applied to claim 1 above, and further in view of Reznik (US Pat. 6,798,040).

Regarding claims 5 and 14, a further difference between Akiyama and the claimed invention is an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer. Figure 1 of Reznik discloses an IGBT with an additional semiconductor layer (buffer layer) 6 between the semiconductor substrate 1 and the base region 4, wherein the impurity concentration of layer 6 is greater than that of the substrate 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Akiyama by including the additional semiconductor layer (buffer layer) of Reznik for the purpose of elevating the charge carrier density in the region, thereby reducing the switching losses (col. 3, lines 4-8).

Claims 1, 2, 3, 6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka.

Regarding claims 2 and 3, Figure 10 of Tanaka discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate 1 of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom); an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region 7 of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate; a first main electrode 11 formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a first semiconductor layer 12 of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer 2B of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second main electrode 3 formed on said first semiconductor layer and said second semiconductor layer; wherein an interface between said second main electrode and each of said first and second semiconductor layers is parallel to said first main surface, a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 microns or smaller (0.8 microns) (paragraph [0187]); a first interface between said first

semiconductor layer 12 and said second main electrode 3 occupies approximately 20-70% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer; and a second interface between said second semiconductor layer 2B and said second main electrode 3 occupies approximately 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer. Tanaka does not specifically disclose a distance between said first main surface and said interface is equal to 200 microns or smaller. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a distance between the first surface and the interface equal to or less than 200 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 6 and 15, Figure 10 of Tanaka discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 10 of Tanaka has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Response to Arguments

Applicant's arguments filed February 6, 2006 have been fully considered but they are not persuasive.

Applicant initially states regarding the interview on October 25, 2005 that "Examiner Landau agreed that the references in the outstanding Office Action do not teach or suggest a substrate having a thickness of 200 μm or less, and having the particular coverage of first and second semiconductor layers on a second electrode of an insulated gate bipolar transistor". In order to clarify the record, it is respectfully noted that the Examiner made no such statement. As indicated in the Interview Summary mailed on 10/25/2005, the Examiner merely stated that the arguments presented would be fully considered when formally submitted. It should also be noted that there were two different 103 rejections for claims 1-3 presented in the previous Office Action. The 103 rejection over Tanaka was not discussed during the interview, nor has Applicant responded to this rejection in any way. Therefore, it would be inaccurate to state that the Examiner agreed the references of record did not teach or suggest the claim limitations.

Applicant argues regarding the combination of Akiyama and Tanaka that "neither reference indicates it would be necessary for a resulting combination to include a substrate having a thickness of less than 200 μm. For example, a combination of these features may result in a substrate as described by Tanaka have a thickness of 220 μm, but including 1 μm thick P-type and N-type layers, as described by Akiyama." It is noted that Tanaka discloses the 1 μm thick layers, not Akiyama. Applicant's argument is based on what "may" result from the combination. Essentially, Applicant has suggested an additional modification to Akiyama, where the thickness of the N- region is increased from 190 μm to 220 μm. It is unclear why Applicant is modifying the N- region in this manner. Is Applicant suggesting that total thickness of the substrate (including the first and second regions) must remain at 220 μm? If so, where in Akiyama is this taught or suggested? Neither Tanka nor Akiyama teach or suggest that when

decreasing the thickness of the first and second regions, the thickness of the N- region must be increased. The Examiner merely suggested modifying the thickness of the first and second regions from 30 μm to less than 1 μm, as stated in the above rejection. There is no apparent reason why the thickness of N- region would change, and certainly no reason why it would increase. Therefore, based on the combination presented by the Examiner, the distance between the first main surface and said interface is less than 200 μm. The examiner has provided a motivation for making the above combination. However, Applicant has not provided any reason for the increase in thickness.

Applicant argues, "the advantages asserted in Reznik are directed to an invention having incompatible goals with the present invention, and therefore one of skill in the art would not have been motivated to combine those features with the invention of Akiyama." The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Applicant further argues "one of skilled in the art would not have been motivated to combine the features described by Reznik with the features described by Akiyama because the purposes of those disclosures are incompatible." Simply because the references may solve different problems does not mean they are incompatible. Both references teach vertical IGBTs; therefore they are drawn to analogous art and are properly combinable. Reznik teaches the specific features of claim 5 (and 14), and also teaches the advantage of having those features (see above rejection). The advantage of having those features applies equally to the device of Akiyama. Therefore, Applicant's arguments are not persuasive.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

April 6, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER